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09/688,045	10/12/2000	Daisuke Sato	107259	5525

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EXAMINER	
MOORE, IAN N	
ART UNIT	**PAPER NUMBER**
2661	9

DATE MAILED: 02/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/688,045	SATO ET AL.	
	Examiner	Art Unit	
	Ian N Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,3-5,9,10,14,15 and 19 is/are rejected.

7)☐ Claim(s) 2,6-8,11-13 and 16-18 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4,7,8.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1,3-5, 9,10,14,15, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muto (U.S. 6,445,718) in view of Calvignac (U.S. 5,557,608).

Regarding claim 1, Muto'718 discloses a data transfer control device (see FIG. 1, Serial Interface Circuit 10) for transferring data among a plurality of nodes that are connected to a bus (see FIG. 2, IEEE 1394 serial Bus, which couples between nodes), the data transfer control device comprising:

a transfer execution circuit (see FIG. 2 Transaction Section Layer circuit 120) that operates when a processing means (see FIG. 1, the combined system of Transaction Controller 126, the Control register 107, and CPU 102) has issued a first start command which instructs continuous packet transfer by hardware (see col. 6, lines 44-56, col. 7, line 59 to col. 8, line 29; note that control registers instructs a startup command/request for data transfer.), for executing processing to divide transfer data into a series of packets and transfer the thus divided series of packets continuously (see FIG. 2, ADP converts/transforms

/divides/ packetizes the data into SBP-2 packets. Link core 101 transmits packets toward the IEEE 1394 bus; see col. 6, lines 44-56; col. 7, lines 59 to col. 8, line 29); and

an arbitration circuit (see FIG. 1, TP I/F 121, SUB CPU 1/F and/or Link Core 101) that operates when the processing means has issued a second start command which instructs packet transfer while continuous packet transfer processing is being executed by the transfer execution circuit, for waiting until one transaction (see col. 7, line 25-51; note that FIFO buffer stores and transfers the packets to the other node, and FIFO buffer is full when it is servicing the first transmission upon the first request/instruction/command. A second start signal is the request packet/signal, which trigger during the FIFO buffer is full. FIFO buffer is full since it is still serving the first transmission. Thus, in response to request/command/ instruction (i.e. second start signal) for data transmission, the transaction controller compares the requested amount of data transmission to the FIFO buffer allocation and hold/suspend/queue the next requested data transmission until the FIFO buffer is not fully occupied (i.e. after completing the first transmission/transaction of packets).)

Muto'718 does not explicitly disclose a processing means instructs first continuous transfer for series of packets; and when the processing means instructs second packet transfer while first continuous packet transfer processing is being executed, for waiting until one transaction or one packet transfer in the first continuous packet transfer has been completed then permitting second packet transfer.

However, the above-mentioned claimed limitations are taught by Calvignac'608. In particular, Calvignac'608 teaches a processing means (see FIG. 1, Traffic Scheduler 20)

instructs first continuous transfer for series of packets (see FIG. 1, Traffic scheduler selects the Non-real time traffic queue; see col. 3, lines 43 to col. 4, lines 67); and

when the processing means instructs second packet transfer while first continuous packet transfer processing is being executed, for waiting until one transaction or one packet transfer in the first continuous packet transfer has been completed then permitting second packet transfer (see FIG. 2, while transmitting non-real time packet at time t1, the real-time packet is selected by the scheduler at time t2. The real time packet has to wait until the end of the time t2 where currently transmitting non-real time traffic frame/packet ends. Then, the non-real time traffic is preempted, and the real time packet is transmitted at time t3. See col. 4, line 50 to col. 5, lines 67).

In view of this, having the system of Muto'718 and then given the teaching of Calvignac'608, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Calvignac'608, by providing a mechanism to hold/preempt transmission of real time packet transmission until the end of the currently transmitted non-real time packet, and preempt the continuous non-real time packet transmission in order to sends high priority packet, as taught by Calvignac'608. The motivation to combine is to obtain the advantages/benefits taught by Calvignac'608 since Calvignac'608 states at col. 2, line 25-42 that such modification would reduce delay incurred by having first to complete transmission of a non-real time traffic, thus increase efficiency in the network.

Regarding claim 3, the combined system of Muto'718 and Calvignac'608 discloses all aspects of the claimed invention set forth in the rejection of Claim 1 as described above, and Muto'718 further teaches wherein the arbitration circuit receives a first start signal that goes active when there is a transfer start request from the transfer execution circuit (see FIG. 2, Write Request from ADP to Link CORE before first packet transmission; see col. 6, lines 49 to col. 8, lines 57);

a second start signal that goes active when there is a transfer start request in accordance with the second start command (see FIG. 3, Read Request from ADP to Link CORE before second packet transmission; see col. 8, lines 60 to col. 10, lines 21), and

a completion signal that goes active at transfer completion (see FIG. 4A, Acknowledge message in IEE 1394); then causes the start of transfer processing in accordance with the first start signal when the second start signal went active after the first start signal had gone active, (see col. 1, lines 25-37; note that per IEEE 1394 Standard, the acknowledge packet/signal must be sent for completion of transaction. Note that no request is being granted due to the insufficient FIFO buffer allocation during the first transmission period, and the second request and transmission are being held until the FIFO buffer has sufficient space.)

causes the start of transfer processing in accordance with the second start signal after the completion signal goes active (see col. 7, line 25-51; note that the read request (i.e. 2nd packet transmission must wait unit FIFO buffer is not fully occupied, that is, after completion of 1st packet transmission. The 1st packet transmission is completed once the acknowledge packet/signal is received.)

Regarding claim 4, the combined system of Muto'718 and Calvignac'608 discloses all aspects of the claimed invention set forth in the rejection of Claim 1 as described above, and Muto'718 further teaches wherein the arbitration circuit receives a first start signal that goes active when there is a transfer start request from the transfer execution circuit (see FIG. 2, Write Request from ADP to Link CORE before first packet transmission; see col. 6, lines 49 to col. 8, lines 57);

a second start signal that goes active when there is a transfer start request in accordance with the second start command (see FIG. 3, Read Request from ADP to Link CORE before second packet transmission; see col. 8, lines 60 to col. 10, lines 21), and

a completion signal that goes active at transfer completion (see FIG. 4A, Acknowledge message in IEE 1394; col. 1, lines 25-37; note that per IEEE 1394 Standard, the acknowledge packet/signal must be sent for completion of transaction. Note that no request is being granted due to the insufficient FIFO buffer allocation during the first transmission period, and the second request and transmission are being held until the FIFO buffer has sufficient space.)

Muto'718 does not explicitly disclose giving priority to transfer processing in accordance with the second start/selecting signal when the first and second start/selecting signals have gone active together.

However, the above-mentioned claimed limitations are taught by Calvignac'608. In particular, Calvignac'608 teaches giving priority to transfer processing in accordance with the second start/selecting signal when the first and second start/selecting signals have gone active

together (see FIG. 1, Real-time, Non-Real time buffers, and Scheduler 20; col. 3, lines 35-30; note that both non-real time traffic (data) and real time (voice and video) packets are queuing in their respective queues waiting to be serviced/selected. The scheduler gives high priority to real-time packets over non-real time packets by selection and servicing the real-time packets.)

In view of this, having the system of Muto'718, then given the teaching of Calvignac'608, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Muto'718 and Calvignac'608, by selecting/commanding and servicing the specified/pre-defined packets/traffic as the high priority for transmission when both type traffics/packets are ready to be serviced, as taught by Calvignac'608, for the same motivation as stated above in Claim 1.

Regarding claim 5, the combined system of Muto'718 and Calvignac'608 discloses all aspects of the claimed invention set forth in the rejection of Claim 1 as described above, and Muto'718 further teaches wherein the arbitration circuit receives a first start signal that goes active when there is a transfer start request from the transfer execution circuit (see FIG. 2, Write Request from ADP to Link CORE before first packet transmission; see col. 6, lines 49 to col. 8, lines 57);

a second start signal that goes active when there is a transfer start request in accordance with the second start command (see FIG. 3, Read Request from ADP to Link CORE before second packet transmission; see col. 8, lines 60 to col. 10, lines 21), and

a completion signal that goes active at transfer completion (see FIG. 4A, Acknowledge message in IEE 1394; col. 1, lines 25-37; note that per IEEE 1394 Standard, the acknowledge packet/signal must be sent for completion of transaction. Note that no request is being granted due to the insufficient FIFO buffer allocation during the first transmission period, and the second request and transmission are being held until the FIFO buffer has sufficient space.)

Muto'718 does not explicitly disclose causing the start of transfer processing in accordance with the second start signal when the first start signal went active after the second start signal had gone active, and causes the start of transfer processing in accordance with the first start signal after the completion signal goes active.

However, the above-mentioned claimed limitations are taught by Calvignac'608. In particular, Calvignac'608 teaches causing the start of transfer processing in accordance with the second start/selecting signal when the first start signal went active after the second start/selecting signal had gone active, and causes the start of transfer processing in accordance with the first start signal after the completion signal goes active (see FIG. 1, Real-time, Non-Real time buffers, and Scheduler 20; col. 3, lines 60-65; note that both non-real time traffic (data) and real time (voice and video) packets are queuing in their respective queues waiting to be serviced/selected. The scheduler gives high priority to real-time packets over non-real time packets by selection and servicing the real-time packets. Moreover, in the case non-preemptive polity, non-real time packets/traffic are only transmitted if there are no the real-time packets waiting to be transmitted. Thus, when real-time packets/traffic are

transmitting, non-real time packets/traffic must wait until the real-time transmission is completed.)

In view of this, having the system of Muto'718, then given the teaching of Calvignac'608, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Muto'718 and Calvignac'608, by selecting/commanding and servicing the specified/pre-defined packets/traffic as a real time for transmission and holding/queuing non-real time traffic until the first transmission is completed, as taught by Calvignac'608, for the same motivation as stated above in Claim 1.

Regarding claim 9, the combined system of Muto'718 and Calvignac'608 discloses all aspects of the claimed invention set forth in the rejection of Claim 1 as described above, and Muto'718 further teaches wherein data transfer is performed in accordance with the IEEE 1394 standard (see FIG. 2, IEEE 1394 serial bus and transmission of SBP2 packets).

Regarding claim 10, the combined system of Muto'718 and Calvignac'608 discloses all aspects of the claimed invention set forth in the rejection of Claim 1 as described above, and Muto'718 further teaches Electronic equipment comprising:

the data transfer control device as defined in claim 1;

a device for performing given processing on data, that has been received from another node via the data transfer control device and the bus (see FIG. 1, Local Processor 40; see col. 4, lines 52-64; col. 2, line 26; note that local processor process data from the other node); and

a device for outputting or storing data that has beer subjected to the processing (see FIG. 1, HDD 30; see col. 4, lines 52-64; col. 2, line 26; note that HDD, hard disk drive, is the storage device that is subjected to the processing.)

Regarding claim 14, the combined system of Muto'718 and Calvignac'608 discloses all aspects of the claimed invention set forth in the rejection of Claims 1 and 9 as described above, and Muto'718 further teaches Electronic equipment comprising:

the data transfer control device as defined in claim 9;

a device for performing given processing on data, that has been received from another node via the data transfer control device and the bus (see FIG. 1, Local Processor 40; see col. 4, lines 52-64; col. 2, line 26; note that local processor process data from other node); and

a device for outputting or storing data that has beer subjected to the processing (see FIG. 1, HDD 30; see col. 4, lines 52-64; col. 2, line 26; note that HDD, hard disk drive, is the storage device that is subjected to the processing.)

Regarding claim 15, the combined system of Muto'718 and Calvignac'608 discloses all aspects of the claimed invention set forth in the rejection of Claim 1 as described above, and Muto'718 further teaches Electronic equipment comprising:

the data transfer control device as defined in claim 1;

a device for performing given processing on data that is to be transferred to another node, via the data transfer control device and the bus (see FIG. 1, Local Processor 40; see

col. 4, lines 52-64; col. 2, line 26; note that local processor process data from other node); and

a device for fetching data to be subjected to the processing (see FIG. 1, HDD Controller 30; see col. 4, lines 52-64; col. 2, line 26; note that HDD Controller, hard disk drive Controller, obtains the data that is subjected to the processing.)

Regarding claim 19, the combined system of Muto'718 and Calvignac'608 discloses all aspects of the claimed invention set forth in the rejection of Claims 1 and 9 as described above, and Muto'718 further teaches Electronic equipment comprising:

the data transfer control device as defined in claim 9;

a device for performing given processing on data that is to be transferred to another node, via the data transfer control device and the bus (see FIG. 1, Local Processor 40; see col. 4, lines 52-64; col. 2, line 26; note that local processor process data from other node); and

a device for fetching data to be subjected to the processing (see FIG. 1, HDD Controller 30; see col. 4, lines 52-64; col. 2, line 26; note that HDD Controller, hard disk drive Controller, obtains the data that is subjected to the processing.)

Allowable Subject Matter

2. Claims 2, 6-8,11-13, and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 703-605-1531. The examiner can normally be reached on M-F: 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 703-305-4798. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ian N Moore
Examiner
Art Unit 2661

INM
2/6/04

Douglas W. Olms

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